FIREBERD®

Operating Manual

V.35/RS-449/X.21
COMBINED DATA INTERFACE MODULE
(MODEL 42522)
OPERATING MANUAL

TTC™
A Dynatech Company

ML# 12650

V.35/RS-449/X.21
COMBINED DATA INTERFACE MODULE
(MODEL 42522)
OPERATING MANUAL

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TELECOMMUNICATIONS TECHNIQUES CORPORATION
20410 Observation Drive
Germantown, MD 20876 USA
Tel: (800) 638-2049 or (301) 353-1550 (MD) Fax: (301) 353-0731

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SECTION 1
GENERAL INFORMATION

1.1 MANUAL SUMMARY

This reference manual describes the set-up procedures, operating instructions, applications, specifications, maintenance, and service information for Telecommunications Techniques Corporation's V.35/RS-449/X.21 Combined Data Interface Module (Model 42522) for use with the FIREBERD 6000 and 4000 Communications Analyzers.

1.2 MODULE OVERVIEW

The V.35/RS-449/X.21 Combined Data Interface Module gives the FIREBERD 6000 and FIREBERD 4000 the ability to test from a V.35, RS-449, or X.21 access point with the same module. This module does all of the following:

- Performs Bit Error Rate (BER) testing on data links that are out of service
- Emulates Data Transmission Equipment (DTE) or Data Communications Equipment (DCE)
- Performs V.54 (in V.35 mode) loopbacks 2 and 3, RS-449 loopbacks RL and LL, and X.21 loopbacks 2a and 3c

1.3 INTERFACE COMPATIBILITY

The V.35/RS-449/X.21 Combined Data Interface Module is designed in accordance with the following specifications and recommendations:

- V.35 - CCITT Recommendation V.35/306, Data Transmission at 48 kb/s using 60 to 108 kHz Group Band Circuits for Wideband Modems.
- 306 - Bell System Technical Reference Publication PUB41304 for 306 Type Wideband Data Sets, and Bell System Technical Reference Publication PUB41450 for Digital Data System (DDS) Data Service Units (DSUs).
- RS-449 - EIA RS-449, November 1977, General Purpose 37-position Interface for DTE and DCE Terminating Equipment Employing Serial Binary Data Interface.
- X.21 - CCITT Recommendation X.21, 1988, revised. Interface Between DTE and DCE for Synchronous Operation on Public Data Network.

1.4 CABLES

The following cables are available for use with the V.35/RS-449/X.21 Combined Data Interface Module. The model numbers listed are the TTC part numbers. Call TTC Customer Service at (800) 638-2049 or (301) 353-1550.

- Model 10214, 6' V.35 cable with 34-pin male connectors
- Model 10419, 10' V.35 cable with 34-pin male connectors
- Model 10417, 10' RS-449 cable with 37-pin D male connectors
- Model 10215, 6' RS-449 cable with 37-pin D male connectors
- Model 31271, 10' X.21 cable with 15-pin male connectors

SECTION 2
INTERFACE DESCRIPTION

2.1 INTRODUCTION

This section describes the physical features of the V.35/RS-449/X.21 Combined Data Interface Module. Included here are a physical description and the module pin assignments.

2.2 PHYSICAL DESCRIPTION

The user interface for the V.35/RS-449/X.21 Combined Data Interface Module has three female connectors: one each for V.35, RS-449, and X.21. The following subsections briefly describe each connector, and list the pin assignments. Figure 2-1 shows the front panel view of this module, along with the locations of these connectors. See Section 3 of this manual for instructions on installing, configuring, and operating this module with your FIREBERD.

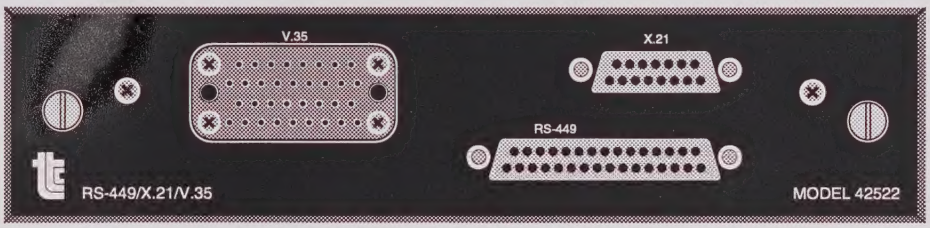


Figure 2-1
V.35/RS-449/X.21 Combined Data Interface Module - Front View

2.2.1 V.35 Interface Connector

The V.35 portion of the V.35/RS-449/X.21 Combined Data Interface Module converts the signal characteristics (as per the interface specifications) to the TTL signals used by the FIREBERD to analyze and test circuit operation. The interface connector is a female, 34-pin connector that allows connection to V.35-compatible equipment. Pin assignments are defined by the CCITT V.35 and Bell 306-type interface standards, and are listed in Table 2-1.

Table 2-1
V.35 Connector Pin Assignments

Pin #:	EIA:	CCITT:	Command:	Signal Source DTE:	Signal Source DCE:	Description:
A	AA	–	PGND	–	–	Protective Ground
B	AB	102	SGND	–	–	Signal Ground
C	CA	105	RS (RTS)	X	–	Request to Send
D	CB	106	CS (CTS)		X	Clear to Send
E	CC	107	DSR		X	Data Set Ready

Table 2-1
V.35 Connector Pin Assignments (Continued)

Pin #:	EIA:	CCITT:	Command:	Signal Source DTE:	Signal Source DCE:	Description:
F	CF	109	RLSD		X	Received Line Signal Detector
H	CD	–	DTR		X	Data Terminal Ready
L			RL	X		Remote Loop
N			LL	X		Local Loop
n			TM		X	Test Mode
P	–	103	SD (A)		X	Send Data (A Lead)
R	–	104	RD (A)		X	Received Data (A Lead)
S	–	103	SD (B)		X	Send Data (B Lead)
T	–	104	RD (B)		X	Received Data (B Lead)
U	–	–	SCTE (A)	X		Serial Clock Transmit External (A Lead)
V	–	115	SCR (A)		X	Serial Clock Receive (A Lead)
W	–	–	SCTE (B)	X		Serial Clock Transmit External (B Lead)
X	–	115	SCR (B)		X	Serial Clock Receive (B Lead)
Y	–	114	SCT (A)		X	Serial Clock Transmit (A Lead)
a	–	114	SCT (B)		X	Serial Clock Transmit (B Lead)
f	–	–	SGND			Signal Ground

2.2.2 RS-449 Interface Connector

The RS-449 portion of the V.35/RS-449/X.21 Combined Data Interface Module converts the signal characteristics (as per the interface specifications) to the TTL signals used by the FIREBERD to analyze and test circuit operation. All clock and data drivers and receivers are high-speed, balanced RS-449 access points. The interface connector is a female, 37-pin type that allows connection to RS-449-compatible equipment. Table 2-2 shows the pin assignments for this connector.

Table 2-2
RS-449 Connector Pin Assignments

37 Pin: A	37 Pin: B	RS-449 Circuit:	Status at Connectors: to DCE:	Status at Connectors: to DTE:	Description:
1		Shield	Shield		
19		SG	Signal Ground		
37		SC	Received Reference		Send Common
20		RC	Received Reference		Receive Common
4	22	SD	X		Send Data
6	24	RD		X	Receive Data
7	25	RS	X		Request to Send
9	27	CS		X	Clear to Send
11	29	DM		X	Data Mode
12	30	TR	X		Terminal Ready
13	31	RR		X	Receiver Ready
17	35	TT	X		Terminal Timing
5	23	ST		X	Send Timing
8	26	RT		X	Receive Timing
10		LL	X		Local Loopback
14		RL	X		Remote Loopback
18		TM		X	Test Mode

2.2.3 X.21 Interface Connector

The X.21 portion of the V.35/RS-449/X.21 Combined Data Interface Module converts the signal characteristics (as per the interface specifications) to the TTL signals used by the FIREBERD to analyze and test circuit operation. All clock and data drivers and receivers are high-speed, balanced X.21 access points. The interface connector is a female, 15-pin D type that allows connection to X.21-compatible equipment. Table 2-3 presents the pin assignments for the X.21 interface connector.

Table 2-3
X.21 Connector Pin Assignments

15 Pin: A	15 Pin: B	X.21 Circuit:	Signal to DCE:	Signal to DTE:	Description:
	8	G			Signal Ground
2	9	T	X		Transmit Data
4	11	R	X		Receive Data
3	10	C		X	Control
5	12	I	X		Indication
6	13	S		X	Signal Element Timing
1					Shield

NOTE: The 15-pin D type (X.21) and the 37-pin (RS-449) connectors are driven in conjunction. Use only one of these connectors at a time with this interface module.

SECTION 3
INSTALLATION AND OPERATION

3.1 INTRODUCTION

This section describes how to install, configure, and operate the V.35/RS-449/X.21 Combined Data Interface Module when it is used in a FIREBERD 6000 or 4000. Refer to the appropriate FIREBERD Reference Manual for specific instructions on operating the FIREBERD mainframe.

NOTE: Be sure to configure your FIREBERD and the V.35/RS-449/X.21 Combined Data Interface Module before connecting to the circuit under test.

3.2 INSTALLING THE INTERFACE MODULE

Figure 3-1 shows the positioning of the V.35/RS-449/X.21 Combined Data Interface Module.

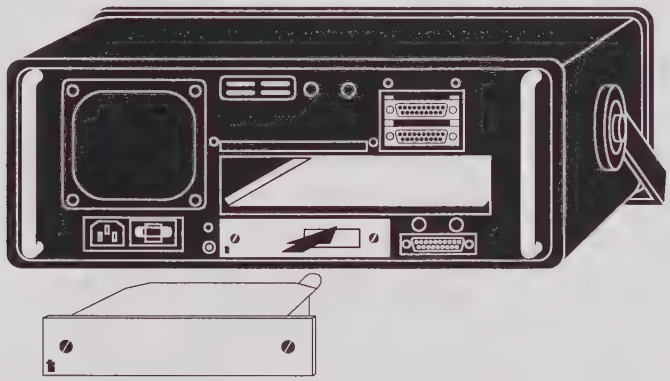


Figure 3-1
FIREBERD Interface Installation

The procedure for installing and configuring an interface module into the FIREBERD 6000 and FIREBERD 4000 are the same. Follow this procedure to install your V.35/RS-449/X.21 Combined Data Interface Module into either a FIREBERD 6000 or 4000:

1. Turn the FIREBERD AC power OFF.

2. Facing the rear panel of the FIREBERD, position the interface module as shown in Figure 3-1, with the module face plate facing out.

3. Slide the interface module into the FIREBERD until the interface panel is flush with the rear panel. Make sure the interface board edges fit into the card guides in the mainframe.

4. Secure the interface with the thumbscrews on the interface panel.

5. Turn the FIREBERD mainframe AC power ON, and configure the FIREBERD and interface module as described in the following sections.

3.3 CONFIGURING THE MODULE FOR FIREBERD OPERATION

To configure your V.35/RS-449/X.21 Combined Data Interface Module for use with your FIREBERD 6000 or 4000, follow this procedure:

1. If not applied, turn on the FIREBERD AC power. If the SELF LOOP indicator is illuminated, press the **SELF LOOP** switch to extinguish the LED in the switch.

2. Press the **GEN CLK** (Generator Clock) switch to select the signal timing source. Note that INTF is used to select both Network Timing (ST) and Terminal Timing (TT).

3. Press the **MENU** switch until the LED next to the INTF SETUP label is illuminated.

4. Press the INTERFACE softkey to select 449V35 for the V.35/RS-449/X.21 Combined Data Interface Module.

5. Use the **MENU** switch to select other test criteria (such as test duration, auxiliary functions, etc.).

6. Connect the interface module to the DTE or DCE device under test using the appropriate data connector.

7. Set the ANALYSIS RESULTS indicators, **ANALYSIS MODE** and **PRINTER** switches as required.

3.3.1 Interface Set-up Review

Access the V.35/RS-449/X.21 Combined Data Interface Module through the INTF SETUP menu on your FIREBERD 6000, and through the INTERFACE menu on the FIREBERD 4000. Pressing the **MORE** key within this menu scrolls you through a list of parameters or indicates help. Table 3-1 lists some basic instructions on setting up an interface module.

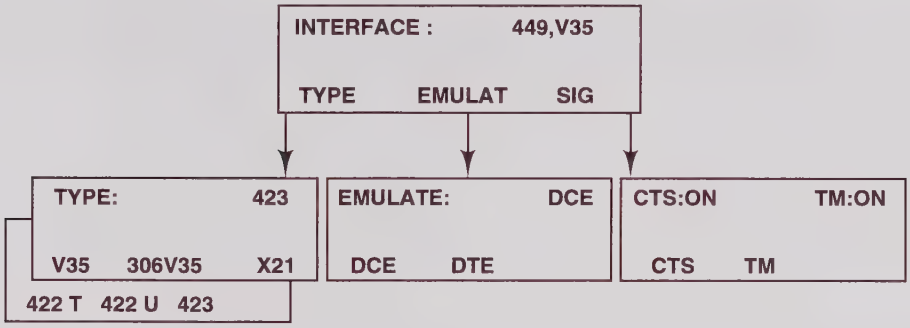
Table 3-1
Interface Set-up Review

To:	Do the Following:
Access the module menu	Press the 449V35 softkey
Select a menu function or select another menu	Press the corresponding softkey
Return to the previous menu display	Press the **UP ARROW** (↑) key on the FIREBERD 6000, **HOME** key on the FIREBERD 4000
Return to the menu's top level	Press the **ENTER** key

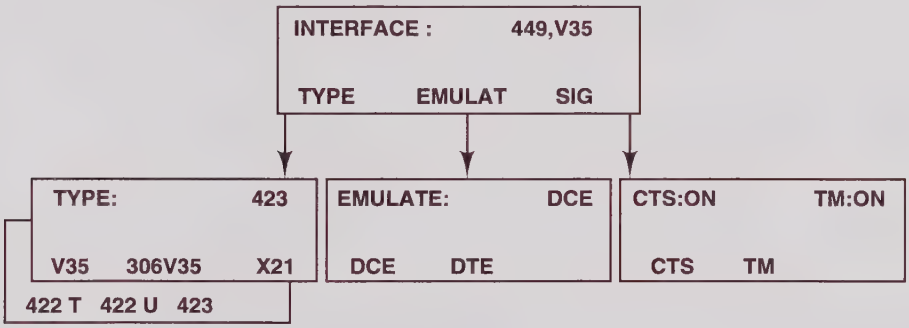
3.4 FIREBERD 6000 MAINFRAME CONFIGURATIONS

This section describes all other configurations of the interface, including FIREBERD 6000 menu selections. This interface supports all of the auxiliary functions of the FIREBERD 6000 mainframe. Figure 3-2 depicts the FIREBERD 6000 user interface menu selections.

For V.35, V.35/306 422 T, 422 U, 423, X.21 DCE Combinations:



For V.35, V.35/306 422 T, 422 U, 423, DTE Combinations:



For X.21 DTE/DCE Combinations:

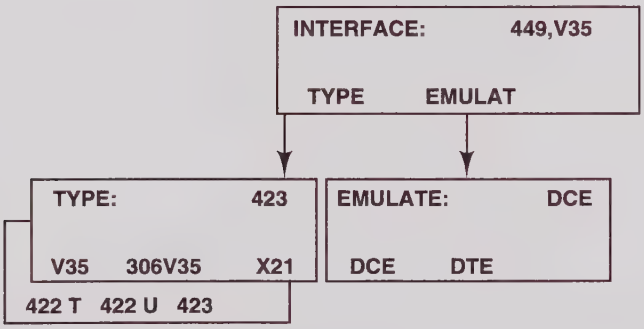


Figure 3-2
FIREBERD 6000 User Interface

3.4.1 FIREBERD 6000 Self Loop

This interface enters Self Loop mode by pressing the **SELF LOOP** switch, and by connecting SD to RD, and TT to RT. To work properly it must receive ST from a valid source (INTF, SYNTH, BNC). This provides quick verification of the FIREBERD and the data interface. User connections do not need to be removed during the test.

3.4.2 FIREBERD 6000 Error Insert

This interface module uses the standard error insert function in the FIREBERD. Error insertion is controlled by using the **ERROR INSERT** switch on the front panel of the FIREBERD.

3.4.3 FIREBERD 6000 Generator Clock

The **GEN CLOCK** switch selects the appropriate clock source to be used during testing: internal (INTRNL), interface (INTF), or external (BNC). This subsection describes generator clock functions for the V.35, RS-449, and X.21 portions of this interface in DTE and DCE emulation.

V.35/306 Interface - V.35 Mode DTE Emulation

When the **GEN CLOCK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock that then generates the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation.

When the **GEN CLOCK** switch is set to INTF, the clock on Pin Y Serial Clock Transmit is used as the transmit timing source for transmitting the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation. Set the generator clock for INTF when the FIREBERD 4000 is emulating DTE.

When the **GEN CLOCK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation.

In all of the above cases, data is received from the DCE on Pin R Receive Data as clocked by Pin V Serial Clock Receive DCE Source.

V.35/306 Interface - 306 Mode DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, that then generates the test pattern on Pin P, Send Data. The external transmit clock used to clock data to the DCE is developed from the internal GEN CLOCK and transmitted to the DCE on Pin U, Serial Clock Transmit External.

When the **GEN CLK** switch is set to INTF, the clock on Pin Y, Serial Clock Transmit is used as the transmit timing source for transmitting the test pattern on Pin P, Send Data. The external transmit clock used to clock data from the DCE is developed from the received interface block and transmitted to the DCE on Pin U, Serial Clock Transmit External. Set the generator clock for INTF when the FIREBERD 4000 is emulating DTE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin P, Send Data. The external transmit clock used to clock data to the DCE is developed from the GEN CLK IN signal and is transmitted to the DCE on Pin U, Serial Clock Transmit External.

In the previous cases, data is received from the DCE on Pin R Receive Data as clocked by Pin V Serial Clock Receive DCE Source.

V.35/306 Interface - V.35 Mode DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, that then generates the test pattern on Pin R, Send Data. The clock source is provided to the DCE Pin V, Serial Clock Receive DCE Source.

When the **GEN CLK** switch is set to INTFC, no clock source is available to provide transmission timing since the DCE, not the interface, acts as timing source. As a result, no data is generated or transmitted.

When the **GEN CLK** switch is set to BNC, the GEN CLOCK IN connector on the rear panel supplies the mainframe with the clock source. This clock is the timing source for transmitting the test pattern data on Pin R, Receive Data. The GEN CLK IN clock source is provided to the DTE on Pin V, Serial Clock Receive DCE Source.

In the previous cases, data is received from the DTE on Pin P, Send Data. The data is received at the DTE using timing based on the clock available at Pin Y, Serial Clock Transmit. The clock at Pin Y, is in phase with the clock provided by the DCE at Pin V (SCR). The source for SCR may be internal to the mainframe or from the external BNC clock input as described above.

V.35/306 Interface - 306 Mode DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, which then generates the test pattern on Pin R, Receive Data. The clock source is provided to the DTE on Pin V Serial Clock Receive DCE Source.

When the **GEN CLK** switch is set to INTF, Pin U, Serial Clock Transmit External supplies the clock source that generates the test pattern on Pin R, Receive Data. This clock is also provided to the DTE on Pin V, Serial Clock Receive DCE Source.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the timing source for transmitting the test pattern data on Pin R, Receive Data. The GEN CLK IN clock source is provided to the DTE on Pin V, Serial Clock Receive DCE Source.

In all of the above cases, data is received from the DTE on Pin P, Send Data using Pin U, Serial Clock Transmit External as the timing source. The data received on Pin P and the clock received on Pin U are developed at the DTE, using timing based on the clock available at Pin Y, Serial Clock Transmit. The clock at Pin Y is in phase with the clock provided by the DCE at Pin V (SCR). The source for SCR may be internal to the mainframe, from the DTE by Pin U of the interface, or from the external BNC clock input as described above.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS (Request To Send) and DTR (Data Terminal Ready) by turning the leads on and off. The status of RLSD (Received Line Signal Detector), DSR (Data Set Ready), TM (Test Mode), and CTS (Clear To Send) are monitored, and are displayed on the front panel.

RS-449 Interface - DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin 4, Send Data and supplies the external transmit clock on Pin 17, Terminal Timing. The DCE transmit clock on Pin 5, Send Timing is ignored when the internal mainframe clock is used.

With **GEN CLK** switch is set to INTF, the clock on Pin 5, Send Timing is the transmit timing source for transmitting the test pattern on Pin 4, Send Data. It also supplies the external transmit clock on Pin 17, Terminal Timing. Typically, the DCE supplies transmit timing to the DTE on Pin 5 and the DTE generates the data (test pattern) from that clock and redistributes the timing signal on Pin 17 to the DCE. Set the generator clock for INTF when the FIREBERD is emulating DTE.

When the **GEN CLK** switch is set for BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin 4, Send Data. In also supplies the external transmit clock on Pin 17, Terminal Timing.

In all of the above cases, the received data is clocked in on Pin 6, Receive Data with the receive clock from the DCE on Pin 8, Receive Timing supplying the timing. Signal analysis is performed on the received data and receive clock signals.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS and DTR by turning the leads off and on. The status of RLSD, DSR, TM, and CTS are monitored and displayed on the front panel.

RS-449 Interface - DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin 6, Receive Data, and supplies the external transmit clock on Pin 8, Receive Timing. The DCE transmit clock on Pin 17, Terminal Timing is ignored when the internal mainframe clock is used.

When the **GEN CLK** switch is set to INTF, the clock on Pin 17, Terminal Timing is used as the transmit timing source for transmitting the test pattern on Pin 6, Receive Data. It also supplies the external transmit clocks on Pin 8, Receive Timing and Pin 5, Send Timing. Typically, the DCE supplies transmit timing to the DTE on Pin 5 and the DTE generates the data (test pattern) from that clock and redistributes the timing signal on Pin 17 to the DCE. Set the generator clock for INTF when the FIREBERD is emulating DTE, not DCE.

When the **GEN CLK** switch is set for BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is used as the timing source for transmitting the test pattern on Pin 6, Receive Data, and also supplies the external transmit clocks on Pin 8, Receive Timing and Pin 5 Send Timing.

In all of the above cases, the received data is clocked in from the DTE on Pin 4, Send Data with the clock provided either on Pin 17, Terminal Timing (TT mode) or by the DCE source clock (ST mode). When ST mode is selected, the clock used to receive data from the DTE is equivalent to that selected by the GEN CLOCK settings described above.

During DCE emulation, the FIREBERD Interface Status and Control panel switches control RLSD, DSR, CTS, and TM by turning the leads on and off. The status of RTS, DTR, LL (Local Loop), and RL (Remote Loop), are monitored and displayed on the FIREBERD front panel.

X.21 Interface - DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which is used to generate the test pattern on Pin 2, Transmitted Data. The DCE transmit clock on Pin 6, Signal Element Timing is ignored when the internal mainframe clock is used.

When the **GEN CLK** switch is set to INTF, the clock on Pin 6, Signal Element Timing is used as the transmit timing source for transmitting the test pattern on Pin 2, Transmit Data. Setting the generator clock for INTF is the recommended selection when the FIREBERD is emulating DTE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin 2, Transmit Data.

In all of the above cases, the received data is clocked in on Pin 4, Receive Data with the receive clock from the DCE on Pin 6, Signal Element Timing supplying the timing. Signal analysis is performed on the received data and receive clock signals.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS (acting as the X.21 Control signal) by turning the lead on and off. The status of RLSD (acting as the X.21 Indicate lead) is monitored and displayed on the FIREBERD front panel.

X.21 Interface - DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, which then generates the test pattern on Pin 4, Receive Data and supplies the external transmit clock on Pin 6, Signal Element Timing.

When the **GEN CLK** switch is set to INTF, no clock is available for transmission of data to the DTE. Typically, the DCE supplies transmit timing to the DTE on Pin 6, Signal Element Timing and the DTE accepts data from the DCE using that clock and generates the data (test pattern) back to the DCE from that clock. Set the generator clock for INTF when the FIREBERD is emulating DTE, not DCE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the timing source for transmitting the test pattern on Pin 4, Receive Data. It also supplies the external transmit clock on Pin 6, Signal Element Timing.

In all of the above cases, the received data is clocked in from the DTE on Pin 2, Transmit Data as timed by the clock provided on Pin 6, Signal Element Timing. There is no TT mode available in X.21 communications. The clock used to send/receive data to/from the DTE is equivalent to that selected by the GEN CLK settings described above.

During DCE emulation, the FIREBERD Interface Status and Control panel switches control RLSD (acting as the X.21 Indicate signal) by turning the lead on and off. The status of RTS (acting as the X.21 Control lead) is monitored and displayed on the FIREBERD front panel.

3.4.4 FIREBERD 6000 Timing

The TIMING menu establishes the timing mode for the mainframe. Pressing the **TIMING MODE** switch selects between SYNC (synchronous), ASYNC (asynchronous), and REC (recovered) timing positions. Modifying TIMING causes a test restart. Timing speeds are as follows:

SYNC:	This interface operates at up to 15 Mb/s.
ASYNC:	This interface operates at up to 20 kb/s.
RECOVERED (optional):	This interface operates at up to 520 kb/s.

3.4.5 FIREBERD 6000 Recall/Store

The RECALL/STORE function in the FIREBERD 6000 is used to store and recall common test set-ups. This interface uses the standard RECALL/STORE function.

3.4.6 FIREBERD 6000 Data

This interface uses the standard DATA menu patterns. Select the data pattern by using the **MORE** and **DATA** keys on the front panel of the FIREBERD 6000.

3.4.7 FIREBERD 6000 RLSD (RR)/RTS/Loop Up

The **RLSD (RR)RTS/LOOP UP** switch controls the state of the Request to Send (RTS) line in DTE emulation and the Receiver Ready (RR) line in DCE emulation.

3.4.8 FIREBERD 6000 DSR (DM)/DTR/Loop Down

The **DSR (DM)/DTR/LOOP DOWN** switch controls the state of the Data Terminal Ready (DTR) line in DTE emulation and the Data Set Ready (DSR or DM) line in DCE emulation.

3.5 FIREBERD 4000 MAINFRAME CONFIGURATIONS

This section describes the FIREBERD 4000 configurations and menu selections. This interface supports all of the auxiliary functions of the FIREBERD 4000 mainframe. Figure 3-3 depicts the FIREBERD 4000 user interface menu selections.

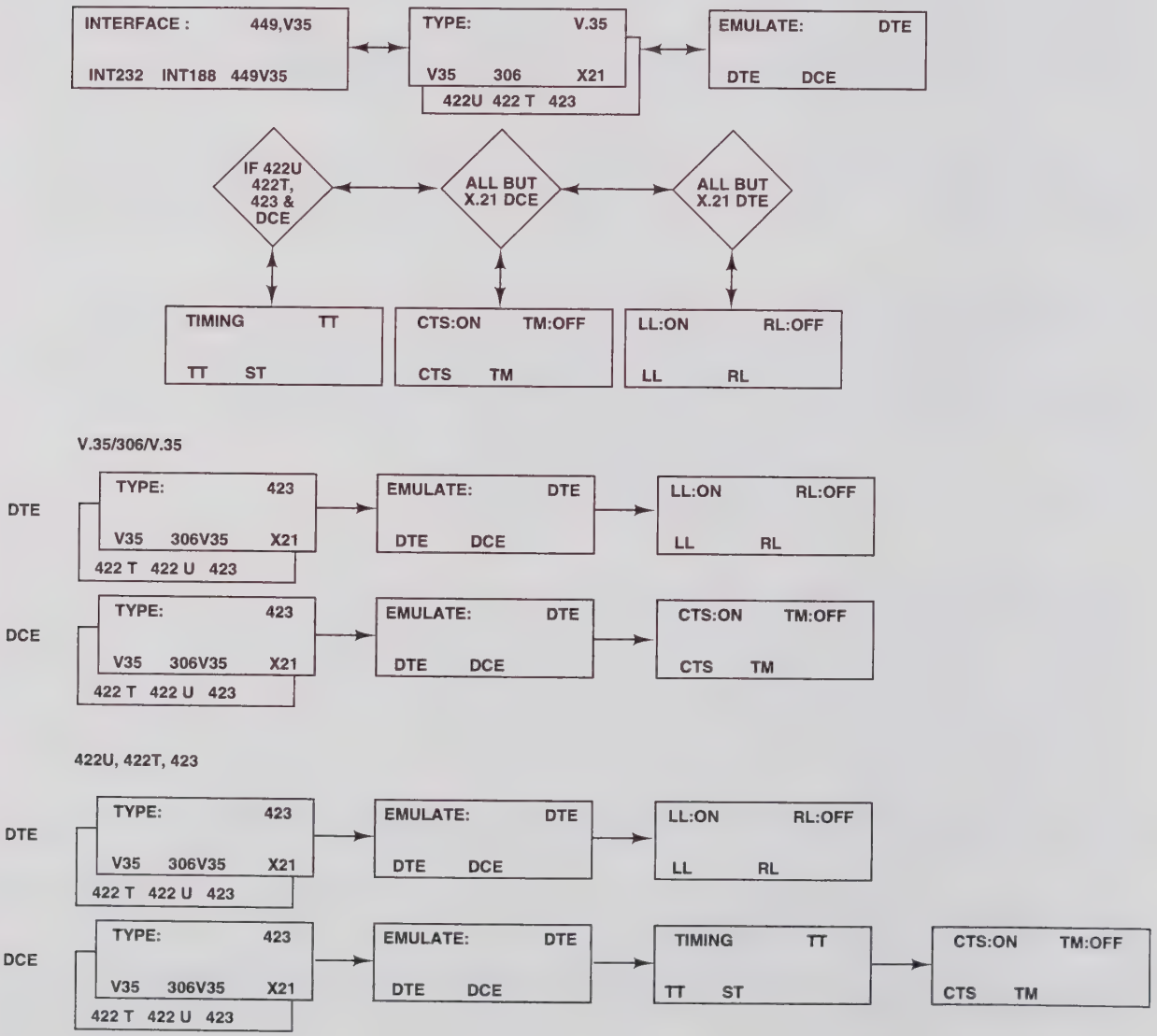


Figure 3-3
FIREBERD 4000 User Interface

3.5.1 FIREBERD 4000 Self Loop

The interface goes through the SELF LOOP mode by pressing the **SELF LOOP** switch, and by connecting SD to RD, and TT to RT. To work properly, the interface must receive ST from a valid source (INTF, SYNTH, or BNC). This provides quick verification of the FIREBERD and the data interface. User connections do not need to be removed during the test.

3.5.2 FIREBERD 4000 Generator Clock

The **GEN CLK** switch selects the appropriate clock source to be used during testing: internal (INTRNL), interface (INTF), or external (BNC). This subsection describes generator clock functions for the V.35, RS-449, and X.21 portions of this interface in DTE and DCE emulation.

V.35/306 Interface - V.35 Mode DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation.

When the **GEN CLK** switch is set to INTF, the clock on Pin Y Serial Clock Transmit is used as the transmit timing source for transmitting the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation. Set the generator clock for INTF when the FIREBERD 4000 is emulating DTE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin P, Send Data. No external transmit clock is supplied back to the DCE in V.35 mode with DTE emulation.

In all of the above cases, data is received from the DCE on Pin R, Receive Data as clocked by Pin V, Serial Clock Receive DCE Source.

V.35/306 Interface - 306 Mode DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin P, Send Data. The external transmit clock used to clock data to the DCE is developed from the internal GEN CLOCK and transmitted to the DCE on Pin U, Serial Clock Transmit External.

When the **GEN CLK** switch is set to INTF, the clock on Pin Y, Serial Clock Transmit is used as the transmit timing source for transmitting the test pattern on Pin P, Send Data. The external transmit clock used to clock data from the DCE is developed from the received interface block and transmitted to the DCE on Pin U, Serial Clock Transmit External. Set the generator clock for INTF when the FIREBERD 4000 is emulating DTE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin P, Send Data to the DCE on Pin U, Serial Clock Transmit External.

In all of the above cases, data is received from the DCE on Pin R, Receive Data as clocked by Pin V, Serial Clock Receive DCE Source.

V.35/306 Interface - V.35 Mode DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, which then generates the test pattern on Pin R, Send Data. The clock source is provided to the DCE Pin V, Serial Clock Receive DCE Source.

When the **GEN CLK** switch is set to INTFC, no clock source is available to provide transmission timing since the DCE, not the interface, acts as timing source. As a result, no data is generated or transmitted.

When the **GEN CLK** switch is set to BNC, the GEN CLOCK IN connector on the rear panel supplies the mainframe with the clock source. This clock is the timing source for transmitting the test pattern data on Pin R, Receive Data. The GEN CLK IN clock source is provided to the DTE on Pin V, Serial Clock Receive DCE Source.

In all of the above cases, data is received from the DTE on Pin P, Send Data. The data received is developed at the DTE using timing based on the clock available at Pin Y, Serial Clock Transmit. The clock at Pin Y is in phase with the clock provided by the DCE at Pin V, Serial Clock Receive. The source for SCR may be internal to the mainframe or from the external BNC clock input as described above.

V.35/306 Interface - 306 Mode DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, which then generates the test pattern on Pin R, Receive Data. The clock source is provided to the DTE on Pin V, Serial Clock Receive DCE Source.

When the **GEN CLK** switch is set to INTF, Pin U, Serial Clock Transmit External supplies the clock source that generates the test pattern on Pin R, Receive Data. This clock is also provided to the DTE on Pin V, Serial Clock Receive DCE Source.

When the **GEN CLK** is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the timing source for transmitting the test pattern data on Pin R, Receive Data. The GEN CLK IN clock source is provided to the DTE on Pin V, Serial Clock Receive DCE Source.

In all of the above cases, data is received from the DTE on Pin P, Send Data using Pin U, Serial Clock Transmit External as the timing source. The data received on Pin P, Send Data and the clock received on Pin U, Serial Clock are developed at the DTE using timing based on the clock available at Pin Y, Serial Clock Transmit. The clock at Pin Y, Serial Clock Transmit is in phase with the clock provided by the DCE at Pin V, Serial Clock Receive. The source for SCR may be internal to the mainframe, from the DTE by Pin U of the interface, or from the external BNC clock input as described above.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS (Request To Send) and DTR (Data Terminal Ready) by turning the leads on and off. The status of RLSD (Received Line Signal Detector), DSR (Data Set Ready), TM (Test Mode), and CTS (Clear To Send) are monitored, and are displayed on the front panel.

RS-449 Interface - DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin 4, Send Data and supplies the external transmit clock on Pin 17, Terminal Timing. The DCE transmit clock on Pin 5, Send Timing is ignored when the internal mainframe clock is used.

With the **GEN CLK** switch is set to INTF, the clock on Pin 5, Send Timing is the transmit timing source for transmitting the test pattern on Pin 4, Send Data. It also supplies the external transmit clock on Pin 17, Terminal Timing. Typically, the DCE supplies transmit timing to the DTE on Pin 5 and the DTE generates the data (test pattern) from that clock and redistributes the timing signal on Pin 17 to the DCE. Set the generator clock for INTF when the FIREBERD is emulating DTE.

When the **GEN CLK** switch is set for BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin 4, Send Data. In also supplies the external transmit clock on Pin 17, Terminal Timing.

In all of the above cases, the received data is clocked in on Pin 6, Receive Data with the receive clock from the DCE on Pin 8, Receive Timing supplying the timing. Signal analysis is performed on the received data and receive clock signals.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS and DTR by turning the leads off and on. The status of RLSD, DSR, TM, and CTS are monitored and displayed on the front panel.

RS-449 Interface - DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which then generates the test pattern on Pin 6, Receive Data, and supplies the external transmit clock on Pin 8, Receive Timing. The DCE transmit clock on Pin 17, Terminal Timing is ignored when the internal mainframe clock is used.

When the **GEN CLK** switch is set to INTF, the clock on Pin 17, Terminal Timing is used as the transmit timing source for transmitting the test pattern on Pin 6, Receive Data. It also supplies the external transmit clocks on Pin 8, Receive Timing and Pin 5, Send Timing. Typically, the DCE supplies transmit timing to the DTE on Pin 5 and the DTE generates the data (test pattern) from that clock and redistributes the timing signal on Pin 17 to the DCE. Set the generator clock for INTF when the FIREBERD is emulating DTE.

When the **GEN CLK** switch is set for BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is used as the timing source for transmitting the test pattern on Pin 6, Receive Data, and also supplies the external transmit clocks on Pin 8, Receive Timing and Pin 5, Send Timing.

In all of the above cases, the received data is clocked in from the DTE on Pin 4, Send Data with the clock provided either on Pin 17, Terminal Timing (TT mode) or by the DCE source clock (ST mode). When ST mode is selected, the clock used to receive data from the DTE is equivalent to that selected by the GEN CLOCK settings described above.

During DCE emulation, the FIREBERD Interface Status and Control panel switches control RLSD, DSR, CTS, and TM by turning the leads on and off. The status of RTS, DTR, LL (Local Loop), and RL (Remote Loop), are monitored and displayed on the FIREBERD front panel.

X.21 Interface - DTE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock which is used to generate the test pattern on Pin 2, Transmitted Data. The DCE transmit clock on Pin 6, Signal Element Timing is ignored when the internal mainframe clock is used.

When the **GEN CLK** switch is set to INTF, the clock on Pin 6, Signal Element Timing is used as the transmit timing source for transmitting the test pattern on Pin 2, Transmit Data. Setting the generator clock for INTF is the recommended selection when the FIREBERD is emulating DTE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the transmit timing source for transmitting the test pattern on Pin 2, Transmit Data.

In all of the above cases, the received data is clocked in on Pin 4, Receive Data with the receive clock from the DCE on Pin 6, Signal Element Timing supplying the timing. Signal analysis is performed on the received data and receive clock signals.

During DTE emulation, the FIREBERD Interface Status and Control panel switches control RTS (acting as the X.21 Control signal) by turning the lead on and off. The status of RLSD (acting as the X.21 Indicate lead) is monitored and displayed on the FIREBERD front panel.

X.21 Interface - DCE Emulation

When the **GEN CLK** switch is set to INTRNL, the mainframe supplies the clock source from the internal generator clock, which then generates the test pattern on Pin 4, Receive Data and supplies the external transmit clock on Pin 6, Signal Element Timing.

When the **GEN CLK** switch is set to INTF, no clock is available for transmission of data to the DTE. Typically, the DCE supplies transmit timing to the DTE on Pin 6, Signal Element Timing and the DTE accepts data from the DCE using that clock and generates the data (test pattern) back to the DCE from that clock. Set the generator clock for INTF when the FIREBERD is emulating DTE, not DCE.

When the **GEN CLK** switch is set to BNC, the mainframe is supplied with the clock source through the GEN CLK IN connector on the rear panel. This clock is the timing source for transmitting the test pattern on Pin 4, Receive Data. It also supplies the external transmit clock on Pin 6, Signal Element Timing.

In all of the above cases, the received data is clocked in from the DTE on Pin 2, Transmit Data as timed by the clock provided on Pin 6, Signal Element Timing. There is no TT mode available in X.21 communications. The clock used to send/receive data to/from the DTE is equivalent to that selected by the generator clock settings described above.

During DCE emulation, the FIREBERD Interface Status and Control panel switches control RLSD (acting as the X.21 Indicate signal) by turning the lead on and off. The status of Request To Send (acting as the X.21 Control lead) is monitored and displayed on the FIREBERD front panel.

3.5.3 FIREBERD 4000 Pattern

This interface uses the standard PATTERN menu. Use the SETUP SELECT functions on the front panel of the FIREBERD 4000, and refer to Section 2 of the *FIREBERD 4000 Reference Manual* for the PATTERN menu.

3.5.4 FIREBERD 4000 Setup Summary

The SETUP SUMMARY follows typical FIREBERD 4000 conventions (which are described in Section 2 of the *FIREBERD 4000 Reference Manual*) and displays the interface name, GENERATOR CLOCK, PATTERN, INTERFACE TYPE, and EMULATE states, and TIMING when available.

3.6 FIREBERD 6000 AND 4000 DEDICATED RESULTS

This section lists the results which appear when using the FIREBERD. Listed separately are results for the FIREBERD 6000 and FIREBERD 4000. These results are defined in the *FIREBERD 6000* and *4000 Reference Manuals.*

3.6.1 FIREBERD 6000 Results

This section lists the results for the FIREBERD 6000.

ERROR	PERFORMANCE	TIME	SIGNAL	T CARRIER	ALARM
AVG BER	% AVL SEC	TIME	RCV FREQ		PAT LOSS
BER	ERR-SES	DATE	GEN FREQ		PWR LOSS
BIT ERRS	BER-SEC	PATL SEC	DELAY††		CLK LOSS
PAT SLIP	GERR SEC	% PATL SEC			CD CHA
CHAR ERR†	G EFS	ELAP SEC			DAT LOSS
BLK ERRS	G % EFS	ERR EAS			
	DEG MIN	E A SEC			
	% DEG MIN	E F EAS			
	SES				
	% SES				
	UNA SEC				
	AVL SEC				

† This result appears in ASYNC only.
†† This result appears in the DTE modes only.

3.6.2 FIREBERD 4000 Results

This section lists the results for the FIREBERD 4000.

ERROR	PERFORMANCE	TIME	SIGNAL	INTERFACE	SUMMARY
AVG BER	% AVL SEC	TIME	RCV FREQ		BIT ERRS
BER	ERR-SES	DATE	GEN FREQ		PAT SLIP
BIT ERRS	BER-SES	PATL SEC	DELAY††		PAT LOSS
PAT SLIP	GERR SEC	% EFS			
PAT LOSS	G EFS	ELAP SEC			
BLK ERRS	G % EFS	TEST SEC			
	DEG MIN	ERR SEC			
	% DEG MIN				
	SES				
	% SES				
	UNA SEC				
	AVL SEC				

†† This result appears in the DTE modes only.

SECTION 4
INDICATORS, ERROR MESSAGES, AND PRINTS

4.1 INTRODUCTION

This section describes all of the status indicators, signaling switches, and error messages that the V.35/RS-449/X.21 Combined Data Interface module affects in both the FIREBERD 6000 and FIREBERD 4000. Listed separately are status indicators that are unique to the FIREBERD 6000, and to the FIREBERD 4000. Also, this section shows controls and results prints for the FIREBERD 6000 and FIREBERD 4000.

4.1.1 Status Indicators and Error Messages

The following Status Indicators and Error Messages are common to both the FIREBERD 6000 and 4000:

RL/(TM)/ALM 2	Illuminates in DTE or DCE with the respective RL or TM lines ON.
(LL)/CTS/ALM 1	Illuminates in DTE or DCE mode with the respective CTS or LL signaling line ON.
RTS/RLSD (RR)/FRM SYNC	Illuminates in DTE or DCE mode with the respective RLSD or RTS signaling lines ON.
DTR/DSR (DM)/CODE	Illuminates in DTE or DCE mode with the respective DTR or DSR signaling line ON.
EMULATE DTE and EMULATE DCE	The appropriate back panel set illuminates for either DTE or DCE modes.
SYNC (PATTERN SYNC)	Reflects the current status of the pattern synchronization.
SYNC LOSS (PATTERN LOSS)	Reflects the status of pattern loss history.

4.1.2 FIREBERD 6000 Status Indicators and Error Messages

The following status indicators and error messages are unique to the FIREBERD 6000.

DATA INVERT	Indicates data inversion with respect to the pattern being transmitted.
CLOCK INVERT	Reflects receive clock status with respect to the receive data.
NO CLOCK	Indicates a receive clock is not present.

4.1.3 FIREBERD 4000 Status Indicators and Error Messages

The following status indicators and error messages are unique to the FIREBERD 4000.

DATA INVERT	Reflects the status of the generator clock.
CLOCK PRES	Reflects the current status of the receive clock.
CLOCK LOSS	Reflects the status of clock loss history.
PATTERN SLIP	Reflects the status of pattern slip detect history.
POWER LOSS	Reflects the status of power loss history.

4.2 FIREBERD 6000 STATUS, CONTROLS, AND RESULTS PRINTS

This section separately lists the status prints, controls prints, and results prints that are applicable to this interface in the FIREBERD 6000.

4.2.1 FIREBERD 6000 Status Prints

The following status prints are applicable to this interface in the FIREBERD 6000.

```
PATTERN SYNC LOSS
PATTERN SYNC ACQUIRED
RECEIVER CLOCK POLARITY CHANGE
CLOCK LOSS
DATA LOSS
POWER UP
G.821 TRANSITIONS
SIGNALING CHANGE
TEST RESTART
OVERFLOW PRINT
NEW CONFIGURATION
```

4.2.2 FIREBERD 6000 Controls Prints

Figure 4-1 is an example of a FIREBERD 6000 controls print for this interface module:

```
CONTROLS                PRINT
12:09:53          02 DEC 92
DATA:                 2^15-1
SELF LOOP:               OFF
TIMING MODE:            SYNC
INTERFACE:
TYPE:                    V35
LL:                      OFF
RTS:                     OFF
TEST INT:          00:00:10
TEST INT PRNT:           OFF
ERROR PRNT:              OFF
ANALY MODE:              CON
BLOCK LENGTH:
DELAY:             DTR/DTR/
XOFF CHARACTER:          13
NONE
PRINT TERM:           CR LF
PRINTER:             RS-232
DATA BITS:                8

SITE:                 Alpha
ERROR INS:              OFF
GEN CLOCK:             INTF
SYN FRQ:          64.0 kHz
RS449/V35
EMULATE:                DTE
RL:                     OFF
DTR:                    OFF
PRINT EVENT:           NORM
SYNC LOSS PRNT:         OFF
TIME PRNT:              OFF
DISPLAY HOLD:           OFF
                  1000 BITS
XON CHARACTER:           11
AUX FUNC IN USE:
PRINT SPEED:           FAST
REMOTE:                NONE
RS-232:
BAUD:                  9600
```

Figure 4-1
FIREBERD 6000 Controls Print

4.2.3 FIREBERD 6000 Results Prints

Figure 4-2 is an example of a FIREBERD 6000 results print for this interface module:

MANUAL	PRINT		
12:08:46	02 DEC 92	SITE ID	Alpha
BIT ERRS	0	AVG BER	0. E-08
BER	0. E-07	BLOCKS	804009
BLK ERRS	0	AVG BLER	0. E-05
PAT SLIP	0	EA SEC	535
ERR EAS	0	EF EAS	535
RCV FREQ	1500001	GEN FREQ	1500001
DELAY		PAT LOSS	0
PATL SEC	0	%PAT SEC	100.00%
DAT LOSS	0	CLK LOSS	0
PWR LOSS	0	C-D CHA	0
ERR-SES	0	BER-SES	0. E-08
GERR SEC	0	G EFS	536
G %EFS	100.00%	UNA SEC	0
AVL SEC	536	%AVL SEC	100.00%
DEG MIN	0	%DEG MIN	0.00%
SES	0	%SES	0.00%
ELAP SEC	547	EMULATE	DTE
RR	OFF	DM	OFF
CS	OFF	TM	OFF
RS	OFF	TR	OFF
IF	RS449/V35		

Figure 4-2
FIREBERD 6000 Results Print

4.3 FIREBERD 4000 STATUS, CONTROLS, AND RESULTS PRINTS

This section separately lists the status prints, controls prints, and results prints that are applicable to this interface in the FIREBERD 4000.

4.3.1 FIREBERD 4000 Status Prints

The following status prints are applicable to this interface in the FIREBERD 4000.

```
PATTERN SYNC LOSS
PATTERN SYNC ACQUIRED
CLOCK LOSS
POWER UP
DATA LOSS
```

4.2.2 FIREBERD 4000 Controls Prints

Figure 4-3 is an example of a FIREBERD 4000 controls print for this interface module:

```
CONTROLS              PRINT          07:04:50 03          NOV 92
PATTERN:             2^15-1          ERROR INSERT:        OFF
SELF LOOP:              OFF          GEN CLOCK:           SYNTH
SYN FRQ:      1500.0 kHz             DISPLAY HOLD:        OFF
SETUP PROGRAM         NO.0
AUXILIARY SETUP:
FLOW TR/DTR:            OFF          FLOW DM/DSR:         OFF
FLOW RS/RTS:            OFF          FLOW CS/CTS:         OFF
FLOW RR/RLSD:           OFF          SYN LOS ACT:         CLEAR
SYN LOS THR:           NORM          USER SYN THR:        10
BLOCK LENGTH:          10^3          PRINT FMT:           LONG
STATUS PRINTS:          OFF          PRINT EVENT:         OFF
INTERFACE SLOT1:                     RS449/V35
TYPE:                   V35          EMULATE:             DCE
RCV CLK:                 ST          TM:                  OFF
RLSD                    OFF          DSR:                 OFF
REMOTE:                NONE          PRINTER:             RS-232
RS-232:                              DATA BITS:           8
BAUD:                  9600          PARITY:              NONE
```

Figure 4-3
FIREBERD 4000 Controls Print

4.3.3 FIREBERD 4000 Results Prints

Figure 4-4 is an example of a FIREBERD 4000 results print for this interface module:

```
MANUAL                PRINT
07:04:05          03 NOV 92          BIT ERRS                0
AVG BER            0.  E-08          BER
PAT SLIP                 0          BLK ERRS                0
BLOCKS              100794          AVG BLER          0.  E-05
PAT LOSS                 0          PATL SEC                0
ERR SEC                  0          G %EFS             100.00%
TEST SEC                67          GEN FREQ           1500000
RCV FREQ           1500000          ERR-SES                 0
BER-SES            0.  E-08          GERR SEC                0
G EFS                   67          %EFS               100.00%
UNA SEC                  0          AVL SEC                67
%AVL SEC           100.00%          DEG MIN                 0
%DEG MIN             0.00%          SES                     0
%SES                 0.00%          ELAP SEC               67
EMULATE               DCE           RS                    OFF
TR                    OFF           LL                    OFF
RL                    OFF           RR                    OFF
DM                    OFF           IF              RS449/V35
```

Figure 4-4
FIREBERD 4000 Results Print

SECTION 5
REMOTE CONTROL COMMAND SYNTAX

5.1 INTRODUCTION

This section lists remote control commands and queries to use with the V.35/RS-449/X.21 Combined Data Interface Module. Refer to Section 4 of the *FIREBERD 6000 Reference Manual*, or Section 4 of the *FIREBERD 4000 Reference Manual* for more detailed instructions on remote control syntax. Listed are some commands with their corresponding queries.

5.1.1 FIREBERD 6000 and 4000 Remote Control Command Syntax

This subsection lists the remote control commands and corresponding queries that are common to the FIREBERD 6000 and 4000. There is one command and query for this interface that is unique to the FIREBERD 6000, it is listed in Section 5.1.2; the commands and queries unique to the FIREBERD 4000 are listed in Section 5.1.3.

INTF:R449V35:EMULATE [DCE,DTE]
INTF:R449V35:EMULATE?
This command and query determines whether the FIREBERD emulates DTE or DCE.

INTF:R449V35:TYPE [V35, 306V35, X21, 422_T, 422_U, 423]
INTF:R449V35:TYPE?
This command and query indicate the interface type: whether RS-449, X.21, or V.35 is being used.

INTF:R449V35:SIGNAL:RL [OFF, ON]
INTF:R449V35:SIGNAL:RL?
This command and query indicate whether the Remote/Local capability is turned on.

INTF:R449V35:SIGNAL:LL [OFF, ON]
INTF:R449V35:SIGNAL:LL?
This command and query indicate the status of the Local Loopback (LL) line.

INTF:R449V35:SIGNAL:TM [OFF, ON]
INTF:R449V35:SIGNAL:TM?
This command and query indicate the status of the Test Mode (TM) line.

5.1.2 FIREBERD 6000 Remote Control Command Syntax

This remote control command and its corresponding query are unique to the FIREBERD 6000:

INTF:R449V35:SIGNAL:CTS [ON, OFF, AUTO]
INTF:R449V35:SIGNAL:CTS?
This command and query indicate the status of the CTS (Clear to Send) control lead.

5.1.3 FIREBERD 4000 Remote Control Command Syntax

These remote control command and their corresponding queries are unique to the FIREBERD 4000:

INTF:R449V35:RCV_CLK_SELECT [TT, ST]
INTF:R449V35:RCV_CLK_SELECT?
This command and query sets the receive clock. Also, this command and query exists only in 422 T, 422 U, and 423 DCE modes.

INTF:R449V35:SIGNAL:CTS [ON, OFF]
INTF:R449V35:SIGNAL:CTS?
This command and query indicate the status of the CTS (Clear to Send) control lead.

5.2 PRINT CAPABILITY

The V.35/RS-449/X.21 Combined Data Interface Module has all the printer capability of any interface used with the FIREBERD 6000 or FIREBERD 4000 Communications Analyzers. See Section 3 of the appropriate FIREBERD Reference Manual for more extensive information on printing capabilities and options.

SECTION 6
APPLICATIONS

6.1 INTRODUCTION

This section describes some typical applications for testing with the V.35/RS-449/X.21 Combined Data Interface Module. Included here are network testing and component testing applications. This section also addresses some basic troubleshooting measures for using this interface module.

6.1.1 Network Testing

Figure 6-1 shows how FIREBERDs can be used end-to-end to verify channel routing and integrity from any network access point. Network components may be looped back locally or remotely (see Section 5 of this manual for remote control syntax). Networks can be sectionalized using the T1/E1 Drop and Insert mode from any T1/E1 network access point.

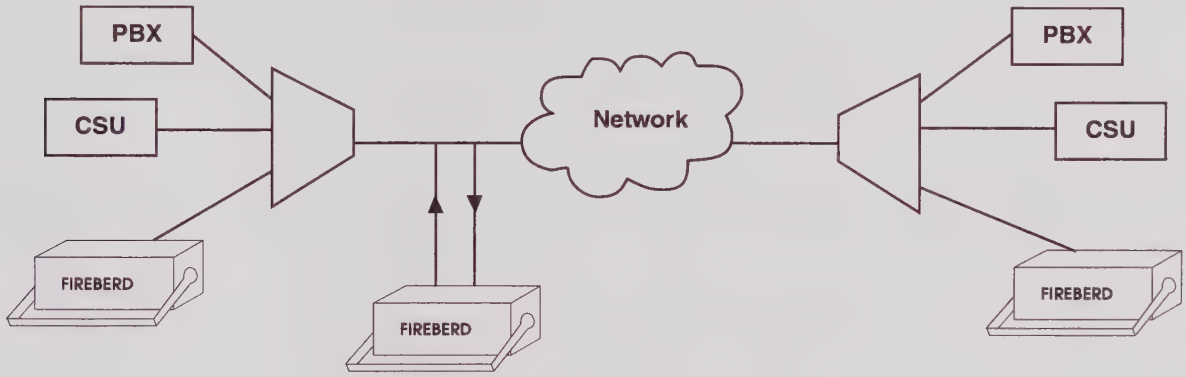


Figure 6-1
Network Testing

6.1.2 Component Testing

Figure 6-2 shows how FIREBERDs can be used to test components from both sides. Built-in stress patterns, loopbacks, and variable transmit levels for T1/E1 make testing components complete. The V.35/RS-449/X.21 Combined Data Interface Module can also be used in automated testing and quality assurance tests.

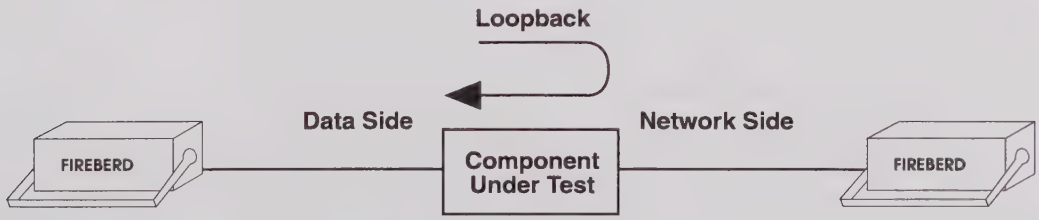


Figure 6-2
Component Testing

6.2 TROUBLESHOOTING GUIDE

This section provides troubleshooting information for the V.35/RS-449/X.21 Combined Data Interface Module. Included are some basic problems that can occur, and some procedures to help you resolve them.

Problem:	Resolution:
No clock indicator illuminated	• Be sure the proper interface type and Emulate mode are selected. • Verify that the CTS, RTS, DTR, and DSR leads are set. • Check cable connections, and ensure that straight-through cables are used.
No SYNC - pattern slips	• Verify the proper timing mode is selected: Synth, INTF - TT or ST. • Verify the proper cabling is used.
Loss of sync at high rates	• Make sure cable is within specified length. The maximum data rate for all interfaces is dependent upon cable length. • For V.35 use 306 mode.
Dribbling errors occur	• Check the Clock-Data Phase Change (C-D CHA) LED indicator on the FIREBERD 6000 to see if the clock is out of phase. • Make sure the proper interface type is selected, and properly connected.
DATA INVERT or CLOCK INVERT detected	• Clear the auxiliary function in use. Use the AUX 99 function.
RL and LL loopbacks do not function	• Make sure the equipment under test is compatible with, and responds to, the loopbacks.
Async framing errors occur	• Check the character format.

SECTION 7
MODULE SPECIFICATIONS

7.1 INTRODUCTION

This section lists the specifications for the V.35/RS-449/X.21 Combined Data Interface Module. Listed separately are the specifications for the V.35, RS-449, and X.21 portions of this interface.

7.1.1 V.35 Interface Specifications

The following are the specifications for the V.35 portion of this interface:

Maximum Data Rate

306 mode:	15 Mb/s
V.35 mode:	dependent upon cable length

Clock and Data Tolerances

Delay, SCT to SD:	70 ns typical
Skew, SCTE to SD:	20 ns typical

Balanced Drivers

Signal Swing (bipolar):	±0.55V ±0.1V into 100Ω
Short circuit current:	less than 100 mA
Rise time:	less than 20 ns
Generator impedance:	100Ω

Balanced Receivers

Load resistance:	100Ω

Polarity

Data polarity:	Mark (binary 1): "A" lead negative with respect to "B" lead Space (binary 0): "A" lead positive with respect to "B" lead
Signaling polarity:	ON: greater than +3VDC OFF: open or less than -3VDC

7.1.2 RS-449 Interface Specifications

The following are the specifications for the RS-449 portion of this interface:

Maximum Speed

RS-449 Balanced: (RS-422)	15 Mb/s synchronous timing 20 kb/s asynchronous timing 520 kb/s recovered timing
RS-449 Unbalanced: (RS-423)	128 kb/s synchronous timing 20 kb/s asynchronous timing 128 kb/s recovered

Polarity

Data polarity:	MARK (binary "1"): "A" lead negative with respect to signal ground SPACE (binary "0"): "A" lead positive with respect to signal ground
Signal polarity:	OFF: "A" lead negative with respect to "B" lead ON: "A" lead positive with respect to"B" lead

Unbalanced Drivers

Short circuit current:	150 mA maximum
Output Level (both states):	0.9Vo (Open circuit voltage, into 450Ω)
Output rise time (clock drivers):	1.2 µs maximum
Output rise time (signaling drivers):	10 µs typical
Open circuit voltage (Vo):	5.5 ±.5 volts

Balanced Drivers

Short circuit current:	150 mA maximum
Differential output signal swing:	2 volts minimum (with a 100Ω load)
Output rise and fall time:	20 ns maximum
Open circuit voltage:	6 volts maximum
Average DC offset:	0V ±0.4 volts

Receivers

Termination resistance: (specified with fail safe networks)	100Ω/unterminated (RCV DATA, RCV CLK, EXT TX CLK)
Input impedance:	7.4 kΩ minimum 6.6 kΩ minimum Single ended A to ground with B grounded
Input threshold:	±0.2 volts (A versus B)

7.1.3 X.21 Interface Specifications

The following are the specifications for the X.21 portion of this interface:

Maximum Speed

X.21:	dependent upon cable length 20 kb/s asynchronous timing 520 kb/s recovered timing

Polarity

Data Polarity:	MARK (binary "1"): "A" lead negative with respect to signal ground SPACE (binary "0"): "A" lead positive with respect to signal ground
Signal Polarity:	OFF: "A" lead negative with respect to "B" lead ON: "A" lead positive with respect to"B" lead

Drivers

Short circuit current:	150 mA maximum
Differential output signal swing:	2 volts minimum (with a 100Ω load)
Output rise and fall time:	20 ns maximum
Open circuit voltage:	6 volts maximum
Average DC offset:	0V ±0.4 volts

Receivers

Termination resistance:	100Ω
(specified with fail safe networks):	(RCV DATA, RCV CLK, EXT TX CLK)
Input Impedance:	7.4 kΩ minimum
	6.6 kΩ minimum
	Single ended A to ground with B grounded
Input threshold:	±0.2 volts (A versus B)

7.2 DIMENSIONS

The following are the dimensions for the V.35/RS-449/X.21 Combined Data Interface Module.

- Width: 7.3 inches (185 mm)
- Height: 1.5 inches (38 mm)
- Depth: 5.2 inches (130 mm)

The Combined Data Interface Module fits into the interface slot for the FIREBERD 6000 and 4000 communications analyzers. Two spring-tensioned screws secure the interface module to the FIREBERD. Connector pins on the module mate with the mainframe's connector receptacle when the interface panel is flush with the mainframe rear panel.

SECTION 8
MAINTENANCE AND SERVICE

8.1 INTRODUCTION

This section contains information on maintenance and service for the V.35/RS-449/X.21 Combined Data Interface Module (Model 42522). It also describes TTC's warranty policy and repair procedures. Any references made to the FIREBERD refer to either the FIREBERD 6000 or 4000 Communications Analyzer, depending upon the users own set-up.

8.2 MAINTENANCE

8.2.1 In Case of Difficulty

If the interface fails to operate and no front panel indicators illuminate, check the following:

- The FIREBERD's AC line power and AC power supply
- AC fuses and fuse rating

If some indicators illuminate and the unit fails to operate:

- Verify that the interface is properly inserted in the FIREBERD. Turn off power before inserting or removing interface.
- Check the interface and/or mainframe cabling and connections to the FIREBERD.
- Substitute another interface, if one is available.

Follow the self-test procedures in the *FIREBERD 6000 Reference Manual* or *FIREBERD 4000 Reference Manual* to localize the problem. If the unit still does not operate, refer to the sections that immediately follow the service information or call the TTC Service Department at (800) 638-2049 or (301) 353-1550 for applications assistance.

NOTE: Verify that the interface clock source is connected before attempting self-test.

8.3 SERVICE

8.3.1 Warranty Policy

All equipment manufactured by Telecommunications Techniques Corporation (TTC) is warranted against defects in material and workmanship. This warranty applies only to the original purchaser and is non-transferrable unless express written authorization of the warranty transfer is granted by TTC.

Liability under this warranty extends ONLY to the replacement value of the equipment. The warranty is void if:

1. Equipment has been altered or repaired without specific authorization from TTC.
2. Equipment is installed or operated other than in accordance with instructions contained in TTC literature and operating manuals.

No other warranty is expressed or implied. TTC is not liable for consequential damages.

8.3.2 In-Warranty Service

Equipment in warranty must be returned to the factory with shipping prepaid. The equipment should be packed and shipped in accordance with the instructions in subsection 8.3.4, Equipment Return Instructions, of this manual. Before returning any equipment, the customer must obtain a Return Authorization (RA) number by contacting the TTC Repair Department. The RA number should then appear on all paperwork and be clearly marked on the outside of the shipping container.

After the equipment is repaired by TTC, it will be tested to ensure it meets applicable specifications, aligned and retested where required, and returned to the customer with shipping prepaid. A brief description of the work performed and the materials used will be provided on the Equipment Repair Report furnished with the returned equipment.

8.3.3 Out-of-Warranty Service

This procedure for repairing out-of-warranty equipment is the same as that used for equipment still in warranty.

However, there is a minimum charge applied to each request for out-of-warranty service. The minimum charge guarantees the customer an estimate of the repair costs and is used as credit against actual materials and labor costs should the equipment be repaired. Contact the TTC Repair Department for specific information on the minimum out-of-warranty repair charge.

The customer will be billed for parts plus standard labor rates in effect at the time of repair. The customer will also be required to furnish a purchase order number before repair work can be started, and TTC must receive a hard copy of the purchase order before the repaired equipment is shipped to the customer. A description of the labor and materials used will be provided in the Equipment Repair Report.

Once an out-of-warranty repair is made, the repaired part or component is warranted for 90 days. This warranty applies only to the part or component that was repaired; other parts or components are not covered under the 90-day repair warranty.

8.3.4 Equipment Return Instructions

The customer should attach a tag to all equipment returned for repair that includes the following information:

1. Owner name and address.
2. A list of equipment being returned and the applicable serial number(s).
3. A detailed description of the problem or service requested.
4. The name and telephone number of the person to contact regarding questions about the repair.
5. The RA number.

If possible, the customer should return the equipment using the original shipping container and material. If the original container is not available, the unit should be carefully packed so that it will not be damaged in transit. TTC is not liable for any damage that may occur during shipping. The customer should clearly mark the TTC-issued RA number on the outside of the package and ship it prepaid and insured to TTC.

Telecommunications Techniques Corporation
20410 Observation Drive
Germantown, MD 20876

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Telecommunications
Techniques
Corporation

Telecommunications Techniques Corporation®
20400 Observation Drive, Germantown, Maryland 20876
Tel. (800) 638-2049 or (301) 353-1550 (MD)
FAX (301) 353-0731